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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,987	02/08/2002	Akira Takekuma	40004101-02	2039

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EXAMINER
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DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/071,987

Applicant(s)

TAKEKUMA, AKIRA

Examiner

Jennifer M. Dolan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 January 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 6-18 is/are rejected.
- 7) ☒ Claim(s) 4, 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 9, 10, 12, 14, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,614,103 to Durocher et al.

Regarding claims 1, 9, 14, and 17, Durocher discloses a LED comprising: a unitary cup (34; figures 11-16); a plurality of electrical traces (37) formed on a surface of the resin cup using an MID means (the cup is made of 3-dimensional molded resin with embedded conductive traces, which makes it an MID structure; see column 3, lines 35-67); a LED chip (59) mounted at the bottom of the cup component (figure 8) and electrically connected to at least a first and second electrical conducting trace (figure 8); and a first connection part (49, 47) connected to the first and second conducting traces for providing electrical connections to external circuitry.

Regarding claim 10, Durocher discloses that the first connection part comprises at least a portion of the first and second leads (figure 11).

Regarding claim 12, Durocher discloses a plurality of LED chips mounted on the cup component (figure 11; 3 chips are mounted on the cup component 31), each having a first and

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second electrode (figures 10 and 11), and 3 or more conducting traces for providing electrical connection to the first and second electrodes (figure 11).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 6-11, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Publication 06-090029 to Itou et al (cited by applicant, hereafter Itou '029) in view of Japanese Patent Publication 07-007185 to Itou (Itou '185)

Regarding claims 1, 6, 9, 14, 17, and 18, Itou '029 discloses a light emitting diode (figure 1) comprising: a cup component (cup portion of 11 and 12); a plurality of electrical conducting traces (11a, 12a metallic layers) formed on a surface of the insulating cup (figures 1 and 2; paragraph 0007) using an MID means (since the cup is formed of 3-dimensional molded resin (see paragraph 0007) with conductive traces printed on the exterior (see figures 1 and 2), it is considered to have an MID construction); a LED chip (13) mounted on the bottom of the cup (figure 1) and electrically connected to first and second traces (figure 1); a first connection part (11c and 12c) connected to the traces for providing electrical connections to external circuitry (paragraphs 0009, 0012, and 0013; it is implicit that since 11c, 11d, 12c, and 12d form a 'leadframe,' they clearly connect to external circuitry. Additionally, the LED would not be functional without connection to some sort of driving circuitry through the leads); and an outer

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mold substantially covering a bottom of the cup component (figure 5; also see figure 1). Insofar as Itou '029 suggests that the two halves of the cup are mechanically joined during fabrication of the assembly, the cup is considered to be unitary (see paragraph 0009). Itou '029, however, fails to specifically state that the cup halves are joined into a unitary body.

Itou '185 teaches a substantially similar assembly wherein an LED chip is deposited into a recess at the bottom of a unitary cup (see figures 1 and 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the cup of Itou '029, such that it is unitary, as taught by Itou '185. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a unitary cup, because both Itou publications show that a chip can be advantageously and equivalently pinched in a recess between a unitary cup or between two cup halves. From a fabrication standpoint, however, it is simpler to provide a unitary cup, since separate cup halves require additional fabrication steps, such as aligning and joining separate cup halves (see Itou '029, paragraph 0009 and Itou '185, paragraph 0007-0009).

Regarding claim 7, Itou '029 discloses conductors (portions of metallic layer connecting 11a to 11c and 12a to 12c) that link to the first and second leads (figure 1).

Regarding claim 8, Itou '029 discloses an extension component (top portions of 17 in figure 4b) extending to the vicinity of the LED chip (figure 4b).

Regarding claim 10, Itou '029 discloses that the first connection part (11c, 12c) is of unitary construction with the first and second traces (portion of the metal layer at 11a and 12a), and thus comprises a portion of the traces.

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Regarding claim 11, Itou '029 discloses conductors (figure 1), which link to an object on which the LED is held.

Regarding claim 15, Itou '029 discloses that the secondary assembly is connected to a lead component (figures 1 and 4; paragraphs 0009-0013).

Regarding claim 16, Itou '029 discloses that a resin mold (14; paragraph 0007) is formed to cover the parts from the outside (figure 1).

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itou '029 in view of Itou '185, as applied to claim 1, supra, and further in view of U.S. Patent No. 5,914,501 to Antle et al.

Itou '029 fails to disclose other electrical components on the surface of the cup and electrically connected to the traces, the other components including a protective element that electrically protects the LED chip.

Antle discloses an LED chip (14) also having a protective element (12) provided in the cup (21), wherein the terminals of the protective element are respectively connected to the two terminals of the LED chip (see figures 2 and 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the LED assembly of Itou '029 in view of Itou '185, such that it includes a protective element, as taught by Antle. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a protective element in the cup, because doing so protects the LED from electrostatic discharge by clamping the applied voltage, thus preventing the LED from being damaged or destroyed by ESD (see

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Antle, column 1, lines 5-67). A person having ordinary skill would further have specified that the protection element be connected to the first and second conducting traces of Itou, because Antle shows that in order for the protection element to function, it must be connected in parallel to the LED chip (Antle, column 1, lines 25-35). Since the terminals of the LED chip are respectively connected to the first and second traces, then the terminals of the protection element must similarly be respectively connected to the first and second traces.

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itou '029 in view of Itou '185, as applied to claim 1, supra, and further in view of U.S. Patent No. 5,564,819 to Yamaguchi.

Itou '029 fails to disclose a plurality of LED chips mounted on the cup, with three or more electrical traces and three or more leads corresponding to the traces.

Yamaguchi discloses an LED structure having two LED chips mounted in the same cup (figures 1 and 5), with each chip having top and bottom electrodes. Yamaguchi further discloses three leads, and wirebonds corresponding to the leads.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Itou '029 as modified by Itou '185, such that a second LED chip, a third trace, and a third lead are provided, as suggested by Yamaguchi. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide a second LED chip in the assembly, because doing so enables a single LED device to emit different colors (see Yamaguchi, column 1, lines 35-55). A person having ordinary skill in the art would then decide to use at least three leads and three traces in the multi-

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LED version of the device of Itou, because using three leads allows for independent operation of the two LED chips, rather than forcing both LEDs to emit simultaneously and at the same voltage. Since the traces are used to connect the LED chips to the leads, there must be at least three traces in order to allow for the independent connection of the LED electrodes to the three leads.

***Allowable Subject Matter***

7. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

8. Applicant's arguments with respect to the rejections using Itou '029 have been considered but are moot in view of the new grounds of rejection. The Applicant did not provide arguments against the rejections using US 6,614,103 to Durocher et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan  
Examiner  
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